EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Scott Tulino (Reg. No. 48317) on July 17, 2008.

The application has been amended as follows:

CLAIM 1 (Currently Amended):

A signal charge transfer line which has been formed on a substrate and is formed to have a number of transfer electrodes, for transferring signal charge by application of transfer pulses to the transfer electrodes via electrode lines, wherein:

the number of transfer electrodes are divided into transfer electrodes of a plurality of sets to each of which a common transfer pulse is applied;

electrode lines for applying common transfer pulses to the transfer electrodes of the plurality of sets are formed on said substrate in common for each of the transfer electrodes of the plurality of sets;

an output gate for outputting the signal charge transferred in the signal charge transfer line is formed on a final part of an output end of the signal charge transfer line; ~~and~~

an electrode line for applying a transfer pulse to a transfer electrode in front of said output gate is inherently formed on said substrate independently of the electrode lines of respective ones of the plurality of sets.

wherein the transfer pulses, which are outputted from two inverting buffer circuits connected in series, are applied to the transfer electrodes of the plurality of sets, and

wherein the transfer pulse, which is outputted from a non-inverting buffer circuit inputting a pulse is outputted from the first inverting buffer circuit of the two inverting buffer circuits.

CLAIM 2 (Currently Amended):

The signal charge transfer line according to claim 1, further including a plurality of drivers provided in correspondence with respective ones of the plurality of sets of the transfer electrodes for applying transfer pulses to the corresponding sets of transfer electrodes;

wherein ~~a~~ the transfer pulse applied by at least one driver among said plurality of drivers is applied to said final transfer electrode in front of said output gate.

CLAIM 4 (Canceled)

CLAIM 5 (Currently Amended):

A signal charge transfer line, comprising:

a plurality of transfer electrodes, wherein a common transfer pulse is applied to each of the plurality of transfer electrodes;

a plurality of electrode lines for applying the common transfer pulse to each of the plurality of transfer electrodes; ~~and~~

an output gate on an output end of the signal charge transfer line, wherein a separate electrode line is connected to a final transfer electrode independently of the plurality of electrode lines.

wherein the separate electrode line applies a transfer pulse to the final transfer electrode independently from the common transfer pulse applied to each of the plurality of electrodes,

wherein the transfer pulses, which are outputted from two inverting buffer circuits connected in series, are applied to the transfer electrodes of the plurality of sets, and

wherein the transfer pulse, which is outputted from a non-inverting buffer circuit inputting a pulse is outputted from the first inverting buffer circuit of the two inverting buffer circuits.

CLAIM 9 (Currently Amended):

The signal charge transfer line according to claim 5, wherein the separate electrode line applies ~~a~~ the transfer pulse only to the final transfer electrode.

CLAIM 10 (Canceled)

CLAIM 11 (Currently Amended):

A signal charge transfer line, comprising:

an electrode line means for applying a common transfer pulse to each ~~or~~ of a plurality of transfer electrodes;

an output gate means for outputting a signal charge transferred in the signal charge transfer line; ~~and~~

a separate electrode line means for applying a transfer pulse to a final transfer electrode, wherein the separate electrode line means is independent of the electrode line means.

wherein the separate electrode line means applies the transfer pulse to the final transfer electrode independently from the common transfer pulse applied to each of the plurality of electrodes,

wherein the transfer pulses, which are outputted from two inverting buffer circuits connected in series, are applied to the transfer electrodes of the plurality of sets, and

wherein the transfer pulse, which is outputted from a non-inverting buffer circuit inputting a pulse is outputted from the first inverting buffer circuit of the two inverting buffer circuits.

CLAIM 15 (Currently Amended):

The signal charge transfer line according to claim 11, wherein the separate electrode line means applies ~~a~~ the transfer pulse only to the final transfer electrode.

CLAIM 17 (Canceled)

CLAIM 20 (Currently Amended):

The signal charge transfer line according to claim 1, wherein the separate electrode line applies the transfer pulse only to ~~a~~ the final transfer electrode.

Allowable Subject Matter

2. **Claims 1-3, 5-9, 11-16, and 18-20** are allowed.

3. The following is an examiner's statement of reasons for allowance:

Claim 1 is allowed because the prior art does not teach or fairly suggest a signal charge transfer line which has been formed on a substrate and is formed to have a number of transfer

electrodes, for transferring signal charge by application of transfer pulses to the transfer electrodes via electrode lines,

wherein the transfer pulses, which are outputted from two inverting buffer circuits connected in series, are applied to the transfer electrodes of the plurality of sets, and

wherein the transfer pulse, which is outputted from a non-inverting buffer circuit inputting a pulse is outputted from the first inverting buffer circuit of the two inverting buffer circuits, ***in combination with the other claimed elements***.

Claims 2-3 and 19-20 are allowed because they each depend on claim 1.

Claim 5 is allowed because the prior art does not teach or fairly suggest a signal charge transfer line,

wherein the transfer pulses, which are outputted from two inverting buffer circuits connected in series, are applied to the transfer electrodes of the plurality of sets, and

wherein the transfer pulse, which is outputted from a non-inverting buffer circuit inputting a pulse is outputted from the first inverting buffer circuit of the two inverting buffer circuits, ***in combination with the other claimed elements***.

Claims 6-9 and 12 are allowed because they each depend on claim 5.

Claim 11 is allowed because the prior art does not teach or fairly suggest a signal charge transfer line,

wherein the transfer pulses, which are outputted from two inverting buffer circuits connected in series, are applied to the transfer electrodes of the plurality of sets, and

wherein the transfer pulse, which is outputted from a non-inverting buffer circuit inputting a pulse is outputted from the first inverting buffer circuit of the two inverting buffer circuits, ***in combination with the other claimed elements***.

Claims 13-16 and 18 are allowed because they each depend on claim 11.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carramah J. Quiett whose telephone number is (571)272-7316. The examiner can normally be reached on 8:00-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NgocYen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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July 17, 2008

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